Wondering how to program your next multi-core? ALMA tool demo @ DATE2014

DRESDEN, - March 25, 2014 – Your next embedded platform will probably have more processor cores than the previous. Do you, as an embedded systems programmer, have the tools to program and exploit the performance of the many cores? At DATE 2014, the ALMA consortium shows how ALMA makes life easier for multi-core programmers with a first demonstration of the ALMA automatic parallelization approach of the ALMA tool chain.

The ALMA tool chain hides the complexity of hardware architectures from the programmer while at the same producing parallel code optimized for the targeted hardware. To achieve that ambitious goal, the ALMA tool-chain uses an abstract description language (ADL) to define target architectures. The ADL description contains the architecture-specific information necessary for parallelizing an application and optimizing code for the target multi-core architectures.

The ALMA tool-chain implements parallelization and optimization algorithms for a whole class of multi-core architectures. The consortium developed ADL descriptions for the embedded reconfigurable multi-core architecture KAHRISMA from Karlsruhe Institute of Technology and for Recore Systems' commercially available many-core processor subsystem IP. ALMA proves the validity of their approach with test applications from the embedded vision and telecommunications domains.

"At DATE2014, we demonstrate the ALMA tool-chain from front-end to the multi-core simulator," explains Timo Stripf from the Karlsruhe Institute of Technology (KIT). "In the ALMA front-end tools we enter an example application for image processing, and we show how the ALMA tool chain translates that into parallelized code which we run on a multi-core architecture in a multi-core simulation environment. Any programmer who tried to parallelize a non-trivial application for multiple cores can confirm that our ALMA tool-chain really reduces the headache."

Today, energy consumption and heat dissipation is the predominant constraint for embedded platforms. "Tomorrow's embedded platforms will rely on heterogeneous many-core processors to provide increased processing performance" says Gerard Rauwerda, CTO at Recore Systems. "Automatic code parallelization is key to the exploitation of the cumulative processing power provided by the many cores. When your new sensors are producing twice as much data, you can basically scale up the number of cores in your many-core subsystem IP and rely on the ALMA tool-chain to compile your software functions to exploit the extra cores."

On the Applied Reconfigurable Computing (ARC) conference next month, the ALMA consortium will explain the tool chain in a special session on ALMA.

About DATE 2014
The DATE conference addresses all aspects of research into technologies for electronic and embedded system engineering. It covers the design process, test, and automation tools for electronics ranging from integrated circuits to distributed embedded systems and addresses both hardware and embedded software design issues. The conference scope also covers design requirements and new architectures for challenging application fields such as telecoms, wireless communications, multimedia, healthcare, smart energy and automotive systems.
www.date-conference.com

ALMA (Greek for 'leap', Αλμα) is an acronym for ALgorithm parallelization for Multicore Architectures. Driven by the technology restrictions in chip design, the end of Moore's law and the quest for increasing computing performance, ALMA is a fundamental step forward in the necessary introduction of novel computing paradigms and methodologies. ALMA strengthens the position of the EU in the world market of multiprocessor targeted software tool chains.
www.alma-project.eu

The ALMA consortium brings together partners from industry and academia. The industry partners Recore Systems and Intracom Telecom contribute their expertise in reconfigurable hardware technology for multi-core systems-on-chip software development tools and real world applications. Five academic partners contribute their outstanding expertise in reconfigurable computing and compilation tools development: Karlsruhe Institute of Technology (KIT, Germany), Université de Rennes I (France), University of Peleponnese (Greece), Technological Educational Institute of Western Greece (Greece) and the Fraunhofer Institute of Optronics, System Technologies and Image Exploitation (Germany).

The ALMA project is supported by the **7th Framework Programme of the European Union** under grant agreement ICT- 287733.

More information: Prof. Dr.-Ing. Dr. h. c. Juergen Becker, Project coordinator, Karlsruhe Institute of Technology – KIT, becker@kit.edu, +49-721 608 42502

Note to editors: If you no longer wish to receive communications about the ALMA project, please unsubscribe here.

More information on the individual partners

Karlsruhe Institute of Technology	http://www.itiv.kit.edu/english/21_53.php
Fraunhofer Institute of Optronics, System Technologies and Image Exploitation	http://www.en.vvs.fraunhofer.de/members/fraunhofer-iosb/

Intracom Telecom	www.intracom-telecom.com
Recore Systems:	www.recoresystems.com
Technological Educational Institute of Western Greece	http://esda-lab.tesyd.teimes.gr
Université de Rennes I	http://www.univ-rennes1.fr/
University of Peleponnese	http://pelopas.uop.gr/UK/